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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/661,037	09/12/2003	John D. Hyde	22524-17802	6704

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EXAMINER	
SOWARD, IDA M	
ART UNIT	PAPER NUMBER
2822	

NOTIFICATION DATE	DELIVERY MODE
03/31/2011	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ptoc@fenwick.com

Office Action Summary	Application No.	Applicant(s)	
	10/661,037	HYDE ET AL.	
	Examiner	Art Unit	
	Ida M. Soward	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 January 2011*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *36,39,40 and 44-51* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *36,39,40,44-48,50 and 51* is/are rejected.

7)☒ Claim(s) *46,48 and 49* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *03/15/2011*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Request for Continued Examination (RCE) filed January 18, 2011.

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: ~~**METHOD AND**~~ **APPARATUS FOR TRIMMING HIGH-RESOLUTION DIGITAL-TO-ANALOG CONVERTER**.

Claim Objections

Claims 46 and 48 are identical. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 36, 44, 45, 46, 47 and 48 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The limitation "**a number of electrons injected into the floating gate *increased responsive to increase* in a voltage difference between the first source**

and the first drain" and "**a number of electrons removed from the second polysilicon floating gate *increase responsive to increase* in voltage at the second drain or the second source**" is unclear.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

As best understood, claims 36, 39-40, 44-48 and 51-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mehta et al. (5,969,992).

In claim 36 Mehta et al. teach a transistor, comprising: a readout transistor, the readout transistor comprising: a n- doped substrate 110 including: a first p- well 180; a first n+ doped region 260 disposed in said first p- well 180 forming a first source; a second n+ doped region 270 disposed in said first p- well 180 forming a first drain; and a channel 280 disposed in said first p- well 180 between said source 260 and said drain 270; a first layer of gate oxide 290 above said channel 280 and said first p- well 180; and a first polysilicon floating gate 340 disposed above said layer of gate oxide 290; and a shorted transistor, the shorted transistor comprising: a n- doped substrate including a second p-well 180, a second drain 200 within the second p-well 180, and a second source 190 within the second p-well 180; a second layer of gate oxide 240 above said first p- well 180; a second polysilicon floating gate 340 above said second layer of gate

oxide 240, the second polysilicon floating gate 340 connected to the first polysilicon floating gate 340; and a conductor connecting the second drain 200 and the second source 190 (Figure 1, columns 3-8, lines 39-67, 1-67, 1-67, 1-67, 1-67 and 1-67, respectively).

In regard to the preamble, If the body of a claim fully and intrinsically sets forth all of the limitations of the claimed invention, and the preamble merely states, for example, the purpose or intended use of the invention, rather than any distinct definition of any of the claimed invention's limitations, then the preamble is not considered a limitation and is of no significance to claim construction. Pitney Bowes, Inc. v. Hewlett-Packard Co., 182 F.3d 1298, 1305, 51 USPQ2d 1161, 1165 (Fed. Cir. 1999). See also Rowe v. Dror, 112 F.3d 473, 478, 42 USPQ2d 1550, 1553 (Fed. Cir. 1997) ("where a patentee defines a structurally complete invention in the claim body and uses the preamble only to state a purpose or intended use for the invention, the preamble is not a claim limitation").

In regard to "for injecting electrons into a floating gate"; "for removing electrons from the floating gate"; "a number of electrons injected into the floating gate increased responsive to increase in a voltage difference between the first source and the first drain" and "a number of electrons removed from the second polysilicon floating gate increase responsive to increase in voltage at the second drain or the second source", claims directed to apparatus must be distinguished from the prior art in terms of structure rather than function, In re Danly, 263, F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). Apparatus claims cover what a device is, not what a device does.

Hewlett-Packard Co. v. Bausch & Lomb Inc., 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

In regard to claims 39 and 51, Mehta et al. teach said readout transistor 130 and the shorted transistor 120 including a single layer on conductive polysilicon 340 (Figure 1, columns 3-8, lines 39-67, 1-67, 1-67, 1-67, 1-67 and 1-67, respectively).

In regard to claims 40 and 52, "even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985). See MPEP § 2113.

In regard to claim 44, Mehta et al. teach a transistor, comprising: a readout transistor 130 comprising: a n- doped substrate 110 including: a first p- well 180; a first n+ doped region 260 disposed in said first p- well 180 forming a first source; a second n+ doped region 270 disposed in said first p- well 180 forming a first drain; and a channel 280 disposed in said first p- well 180 between said source 260 and said drain 270; a first layer of gate oxide 290 above said channel 280 and said first p- well 180; and a first polysilicon floating gate 340 disposed above said layer of gate oxide 290; and a shorted transistor 120 comprising: an n- doped substrate 110 including a second p-well 180, a second drain 200 within the second p-well 180, and a second source 190 within the second p-well 180; a second layer of gate oxide 240 above said first p- well

180; a second polysilicon floating gate 340 above said second layer of gate oxide 240, the second polysilicon floating gate 340 connected to the first polysilicon floating gate 340; a conductor connecting the second drain 200 and the second source 190; and a well contact terminal 210 electrically coupled to said second n- well 180 (Figure 1, columns 3-8, lines 39-67, 1-67, 1-67, 1-67, 1-67 and 1-67, respectively).

In regard to "wherein said synapse transistor is configured to operate as a current source without gate input using a single polysilicon gate layer", claims directed to apparatus must be distinguished from the prior art in terms of structure rather than function, In re Danly, 263, F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). Apparatus claims cover what a device is, not what a device does. Hewlett-Packard Co. v. Bausch & Lomb Inc., 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

In regard to claim 45, Mehta et al. teach a system on a chip (SOC) the system comprising: a pFET synapse transistor including: a readout transistor: an n- doped substrate 110 including; a first p- well 180; a first n+ doped region 260 disposed in said first p- well 180 forming a first source; a second n+ doped region 270 disposed in said first p- well 180 forming a first drain; and a channel 280 disposed in said first p- well 180 between said source 260 and said drain 270; a first layer of gate oxide 290 above said channel 280 and said first p- well 180; and a first polysilicon floating gate 340 disposed above said layer of gate oxide 290; and a shorted transistor 120 comprising: an n-doped substrate 110 including a second n-well 180, a second drain 200 within the second p-well 180, and a second source 190 within the second p-well 180; a second layer of gate oxide 240 above said first p- well 180; a second polysilicon floating gate

340 above said second layer of gate oxide 240, the second polysilicon floating gate 340 connected to the first polysilicon floating gate 340; and a conductor connecting the second drain 200 and the second source 190 (Figure 1, columns 3-8, lines 39-67, 1-67, 1-67, 1-67, 1-67 and 1-67, respectively).

In regard to claims 46 and 48, Mehta et al. teach a n-channel floating-gate device, comprising: a readout transistor 130 comprising: an n- doped substrate 110including: a first p- well 180; a first n+ doped region 260 disposed in said first p- well 180 forming a first source; a second n+ doped region 270 disposed in said first p- well 180 forming a first drain; and a channel 280 disposed in said first p- well 180 between said source 260 and said drain 270; a first layer of gate oxide 290 above said channel 280 and said first p- well 180; and a first polysilicon floating gate 340 disposed above said layer of gate oxide 290; and a shorted transistor 120 comprising: an n- doped substrate 110 including a second p-well 180, a second drain 200 within the second p-well 180, and a second source 190 within the second p-well 180; a second layer of gate oxide 240 above said first p- well 180; a second polysilicon floating gate 340 above said second layer of gate oxide 240, the second polysilicon floating gate 340 connected to the first polysilicon floating gate 340; and a conductor connecting the second drain 200 and the second source 190 (Figure 1, columns 3-8, lines 39-67, 1-67, 1-67, 1-67, 1-67 and 1-67, respectively).

In regard to claim 47, Mehta et al. teach a system on a chip (SOC), the system comprising: a readout transistor 130 comprising: a n- doped substrate 110 including: a first p- well 180; a first n+ doped region 260 disposed in said first p- well 180 forming a

first source; a second n+ doped region 270 disposed in said first p- well 180 forming a first drain; and a channel 280 disposed in said first p- well 180 between said source 260 and said drain 270; a first layer of gate oxide 290 above said channel 280 and said first p- well 180; and a first polysilicon floating gate 340 disposed above said layer of gate oxide 290; and a shorted transistor 120 comprising: an n- doped substrate 110 including a second p-well 180, a second drain 200 within the second p-well 180, and a second source 190 within the second p-well 180; a second layer of gate oxide 240 above said first p- well 180; a second polysilicon floating gate 340 above said second layer of gate oxide 240, the second polysilicon floating gate 340 connected to the first polysilicon floating gate 340; and a conductor connecting the second drain 200 and the second source 190 (Figure 1, columns 3-8, lines 39-67, 1-67, 1-67, 1-67, 1-67 and 1-67, respectively).

However, Mehta et al. fail to the conductivity type regions of the claimed invention.

It is within the level of ordinary skill the interchange types (from n to p or from p to n).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to interchange conductivity type of Mehta et al. to obtain the desired electrical characteristics.

Allowable Subject Matter

Claim 49 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to transistor devices:

Chen et al. (US 6,249,459 B1)

Groeseneken et al. (US 6,570,226 B1)

Ker et al. (5,754,380)

Ker et al. (5,754,381)

Kuo et al. (6,067,254)

Niguyen et al. (US 2001/0015449 A1)

Song (5,616,942)

Tailliet (5,438,213)

Wada et al. (6,144,080).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M. Soward whose telephone number is 571-272-1845. The examiner can normally be reached on Monday - Thursday 6:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra V. Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

IMS
March 28, 2011
/Ida M Soward/
Primary Examiner, Art Unit 2822